Abstract

A compiler for multiple processor and distributed memory architectures is described. The compiler uses a high-level language to represent a task-level network of behaviors that describes an embedded system. The compiler maps a plurality of tasks and data onto a multiple processor, distributed memory hardware architecture. The mapping includes describing a task-level network of behaviors, each of the task-level network of behaviors being related through control and data flow. The mapping further includes predicting a schedule of tasks for the task-level network of behaviors and allocating the plurality of tasks and data to at least one of the multiple processors and to at least one of distributed memory, respectively, in response to the predicted schedule of tasks.